RECEIVED **CENTRAL FAX CENTER**

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

FEB 0 3 2005

Applicants:

Masahiro Ishida, et al.

Scrial No.:

09/699,077

Filing Date:

October 27, 2000

Title:

Method and Apparatus for

Fault Simulation of

Semiconductor Integrated

Circuit

Conf. No.

9031

Examiner: Ayal I. Sharon

Art Unit: 2123

February 3, 2005 San Francisco, California

Commissioner of Patents P.O. Box 1450 Alexandra, VA 22313-1450

RESPONSE TO OFFICE ACTION

Sir:

This communication is submitted in response to the office action mailed November 3, 2004 (referred to herein as "Office Action").